REMARKS

The claims are claims 1, 3, 9, 10, 12 and 18 to 20.

Claims 1, 10, 19 and 20 have been amended to further clarify the subject matter.

Claims 1, 9, 10, 12, and 18 to 20 were rejected under 35 U.S.C. 102(e) as anticipated by Hansen et al U.S. Published Patent Application No. 2003/0110197 Al.

Claims 1, 10, 19 and 20 recite subject matter not anticipated by Hansen et al. Claims 1, 10, 19 and 20 each recite critical paths and that first cells include critical paths and second cells do not. Claims 1 and 19 each recite that "said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than said longest amount of time." Claims 10 and 20 include similar recitations relative to a parallel multiplier core. Hansen et al includes no teaching regarding such critical paths. Accordingly, claims 1, 10, 19 and 20 are allowable over Hansen et al.

Claims 1, 10, 19 and 20 recite further subject matter not anticipated by Hansen et al. Claims 1 and 10 recite first and second cells that are "structurally the same." Claims 1 and 10 recite that "a width of at least one of said first plurality of transistors" forming the first cells "is greater than a width of a corresponding one of said second plurality of transistors" forming the corresponding second cells. Claims 19 and 20 recite that the first Wallace tree cells are structurally the same as the second

Wallace tree cells and that the first Booth decoder cells are structurally the same as the second Booth decoder cells. Claims 19 and 20 each recite that the first plurality of transistors of the first cells are a first width and that the corresponding second plurality of transistors of the corresponding second cells are a second smaller width. Thus claims 1, 10, 19 and 20 each recite cells that are structurally the same with corresponding transistors having differing transistor widths dependent upon whether the cell is within a critical path. Hansen et al neither teaches the width of a transistor difference nor teaches cells differing in any way dependent upon whether they are in a critical path. Therefore Hansen cannot anticipate this limitation of claims 1 and 10.

The FINAL REJECTION states in the Response to Arguments at page 5, line 8 to page 6, line 4:

> "a. The applicant argues in page 9 for independent claims that the cited reference by Hansen et al. does not disclose critical paths as cited in the claimed invention.
>
> "The examiner respectfully submits that there are multiple critical paths within the structure of this MAC. At least one critical paths is longest which can be set as the longest amount of time and at least one critical paths is shortest which can be set as the predetermined time. Thus, any other critical paths in between the shortest and longest critical paths meet the claimed invention.
>
> "b. The applicant argues in pages 10-11 for independent claims that the cited reference by Hansen et al. fails to disclose the differing transistor widths dependent upon whether the cell is within a critical path. In addition, the predetermined time and the width of the first and second Wallace transistors are tied together as critical path.
>
> "The examiner respectfully submits that the language of independent claims do not define or disclose clearly the relationship between the predetermined time involving critical path and the differing width of transistors as argued by the applicant."

While the Examiner is correct that the predetermined time can be chosen arbitrarily small and that "it is impossible to manufacture all transistors with the same width," these arguments fail to take into account that the "predetermined time" limitation and the first and second width limitations are tied together in this invention. Claims 1 and 10 recite first transistors having the first width in Wallace tree cells or Booth decoder cells in a critical path as defined by the predetermined time. Claims 1 and 10 also recite second transistors having the second width in Wallace tree cells or Booth decoder cells "not disposed on any of said at least one critical path." These claims thus require the wider transistors to be in a critical path and the narrower transistors not be in a critical path. This language thus clearly discloses or defines "the relationship between the predetermined time involving critical path and the differing width of transistors" contrary to the assertion of the Examiner. Method claims 19 and 20 include similar limitations.

The FINAL REJECTION including the Response to Arguments fails to point out where Hansen et al teaches this particularly claimed relationship between the predetermined time and the transistor width. The recited predetermined time divides the critical paths from non-critical paths. As recited in the claims, critical paths are always longer in time than non-critical paths. The claims also require that a first transistor in a first Wallace tree cell and in a first Booth decoder cell is greater in width than a corresponding second transistor in a second Wallace tree cell and in a second Booth decoder cell. This is according to the teachings in paragraph [0008], [0009], [0031] to [0037]. In accordance with the teachings in the application, the critical paths would use the wider transistors which are faster but use more power. The non-critical paths would use the narrower transistors which are slower but use less power. In aggregate, this would make the circuit

faster and use less power than using same sized transistors in all paths. Hansen et al fails to teach this relationship between the predetermined time defining which paths are critical and which are non-critical and the transistor widths. Accordingly, claims 1, 10, 19 and 20 are allowable over Hansen et al.

Claims 9 and 18 recite subject matter not anticipated by Hansen et al. Claims 9 and 18 recite "said at least one second cell is a most significant bit or a least significant bit and said at least one first cell is not a most significant bit or a least significant bit." Respective base claims 1 and 10 recite that first cells include a critical path and second cells do not. Hansen et al includes no teaching regarding critical paths and no teaching that most significant bits or least significant bits are not a critical path (second cells) and that paths not the most significant bits nor the least significant bits are the critical path (first cells). While Hansen inherently includes most significant bit cells and least significant bit cells, Hanson fails to teach such cells are constructed with the different widths for corresponding transistors as recited in respective base claims 1 and 10. Accordingly, claims 9 and 18 are allowable over Hansen et al.

Paragraph 5 on page 5 of the FINAL REJECTION states that claims 3 and 12 are allowable but dependent upon a rejected base claim. The Applicants respectfully submit that the above arguments show that base claims 1 and 10 are allowable. Thus claims 3 and 12 are allowable.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

/Robert D. Marshall, Jr/
Robert D. Marshall, Jr.
Reg. No. 28,527